Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. 1CLR**
2. **1D**
3. **N/C**
4. **1CLK**
5. **N. 1PRE**
6. **1Q**
7. **N. 1Q**
8. **GND**
9. **N. 2Q**
10. **2Q**
11. **N. 2PRE**
12. **2CLK**
13. **N/C**
14. **2D**
15. **N. 2CLR**
16. **VCC**

**.055”**

**5 4 3**

**6**

**7**

**8**

**9**

**10**

**11 12 13**

**2**

**1**

**16**

**15**

**14**

**MASK**

**REF**

**ACT74**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: ACT74**

**APPROVED BY: DK DIE SIZE .055” X .055” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ACT74**

**DG 10.1.2**

#### Rev B, 7/1